Enhancement-mode BEOL In_2O_3 FETs with Record Logic Performance: Experiments and Compact Modeling

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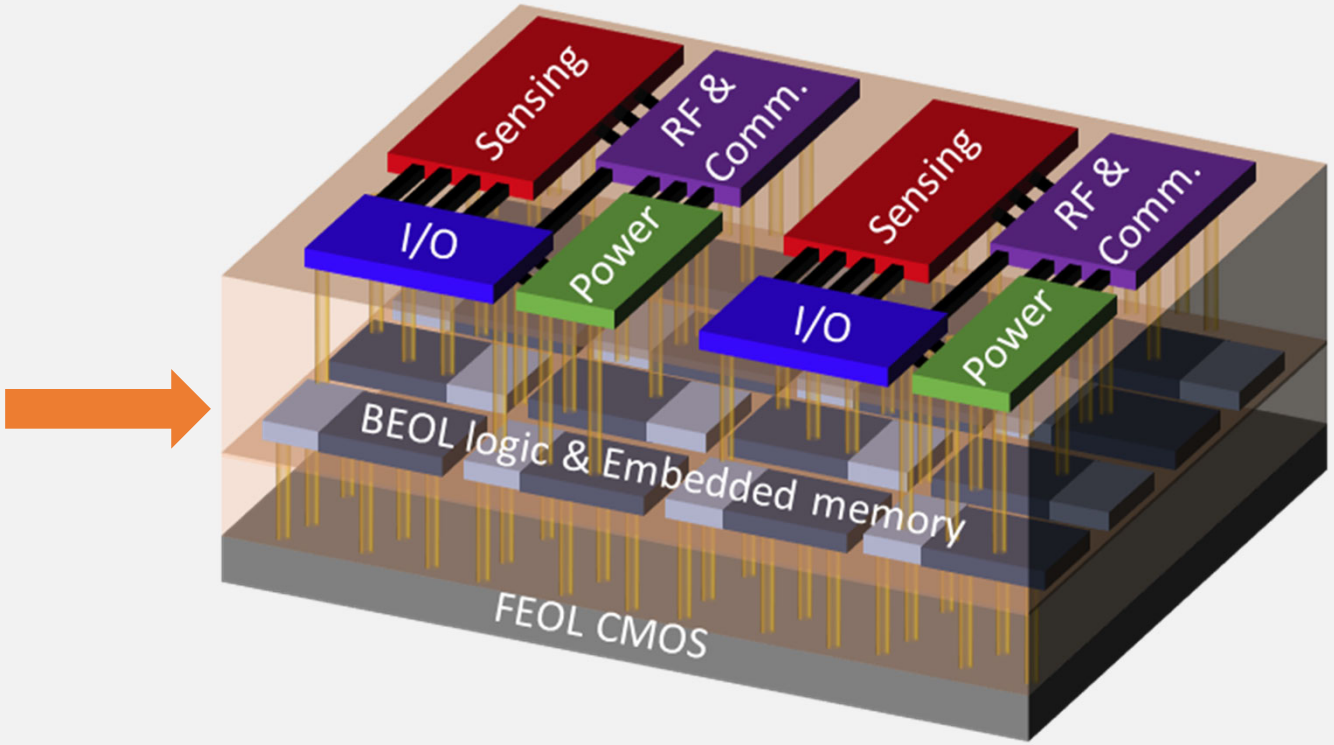
Sponsorship: SRC & Intel & NSERC & CRC

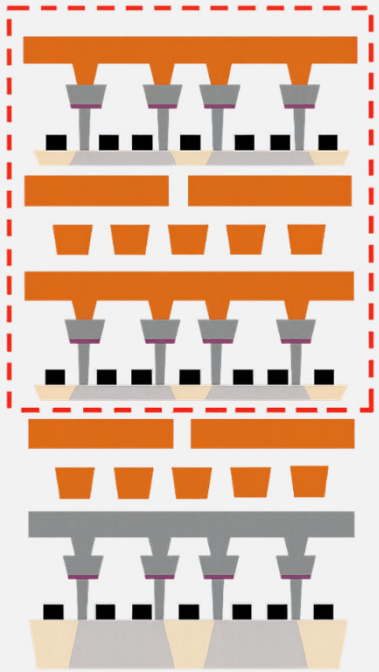
Achieving dramatic energy efficiency improvement

Approach: back-end functionality integration



- Enhanced information throughput
- High system density

Challenge: thermal budget



New transistors and memory with low thermal budget (≤ 400 °C)

Low-k and interconnect (≤ 400 °C)

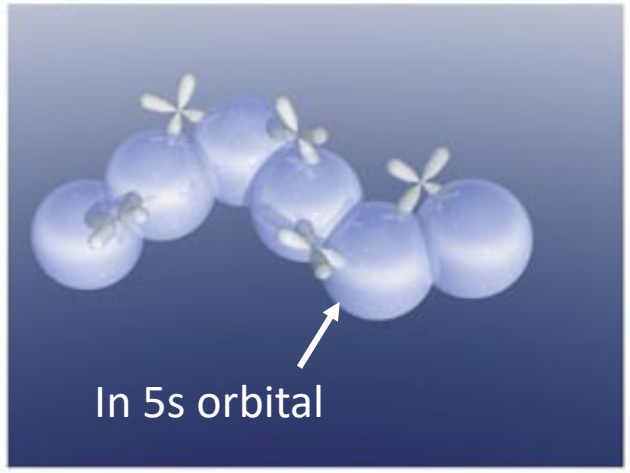
Front-end CMOS (> 900 °C)

Thean, *IEDM* 2022

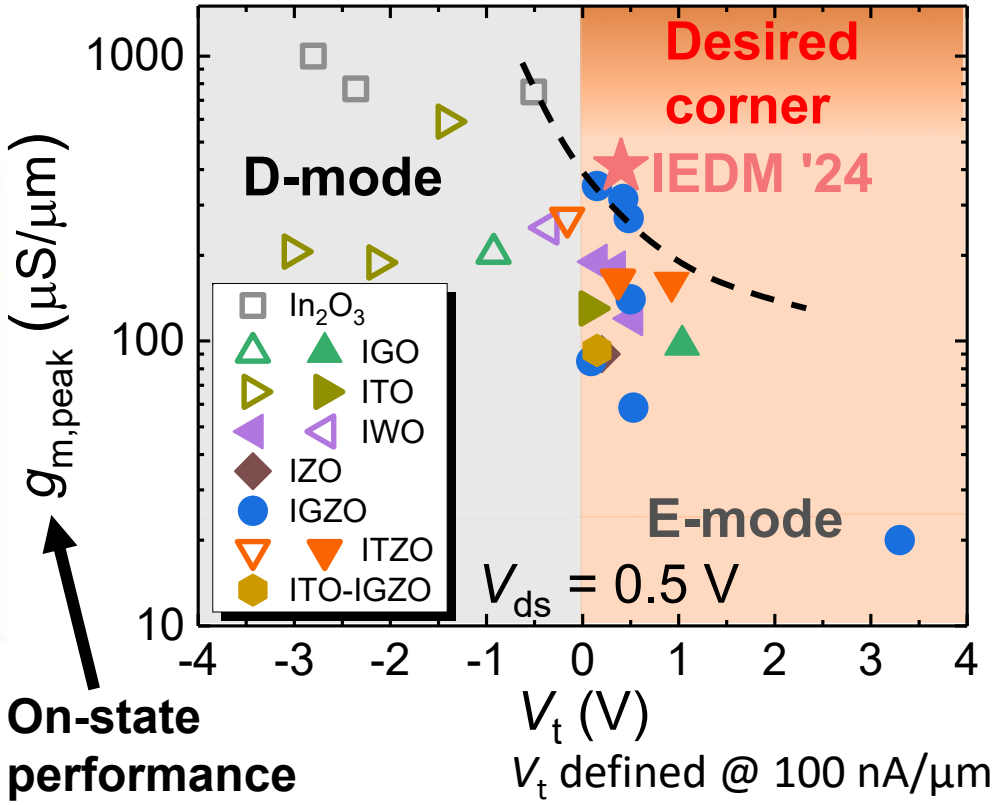
- CMOS-compatible thermal budget (≤ 400 °C) and process

BEOL FETs with amorphous oxide semiconductors

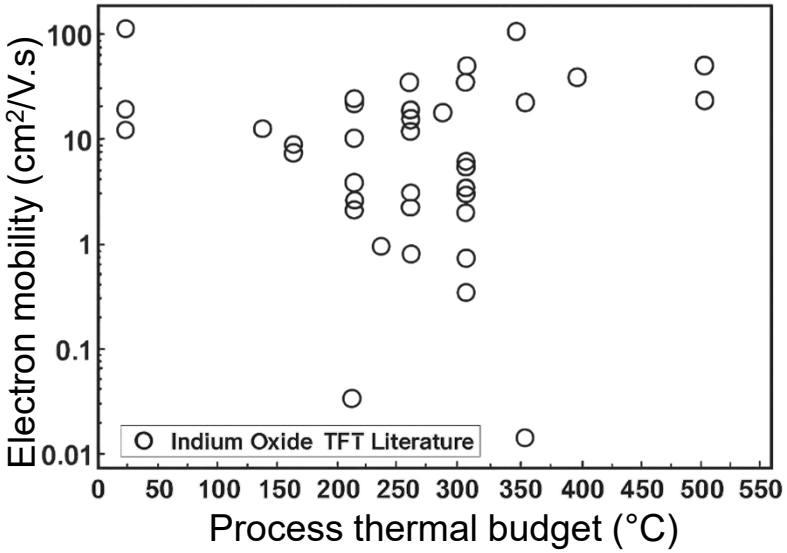
In-based amorphous oxide semiconductor (AOS)



Nomura, *Nature* 2004



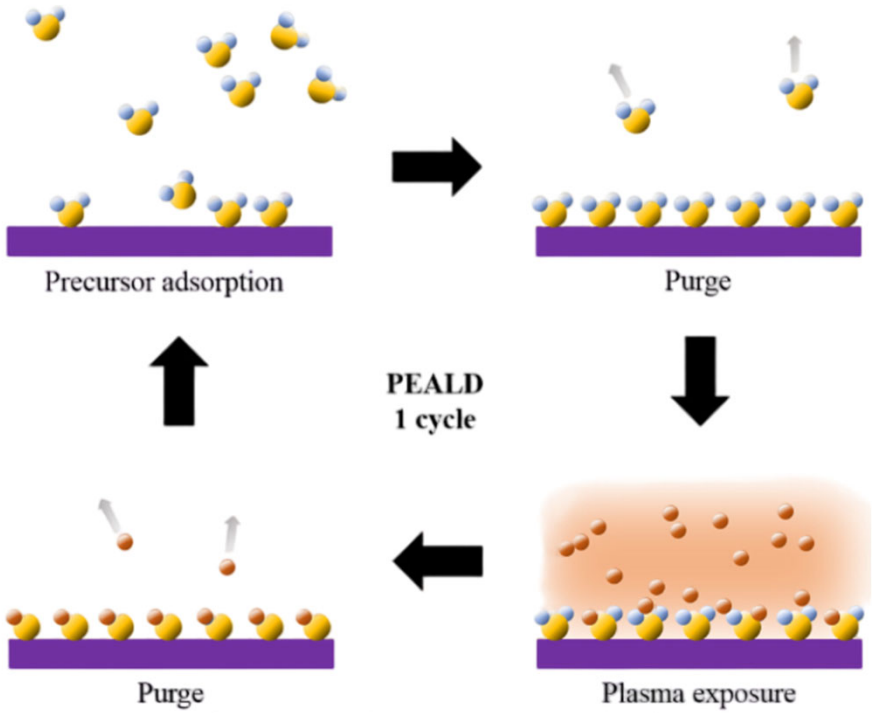
In_2O_3 mobility insensitive to thermal budget



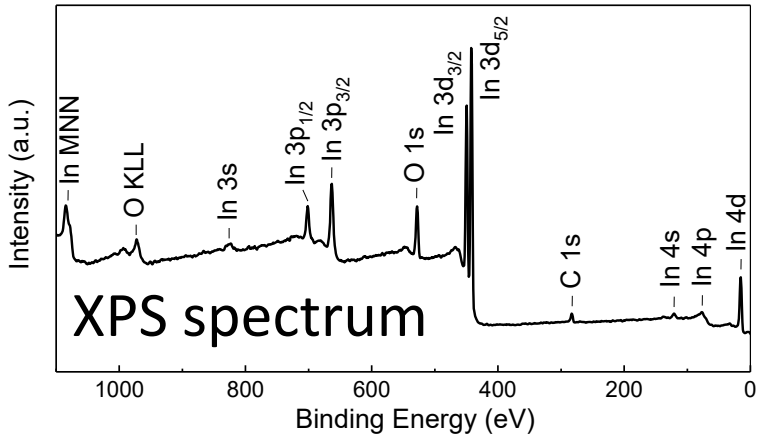
Charnas, *Adv. Mater.* 2024

- Decent mobility in In-based amorphous oxide
- Goal: In_2O_3 FETs with E-mode and high performance, at low thermal budget

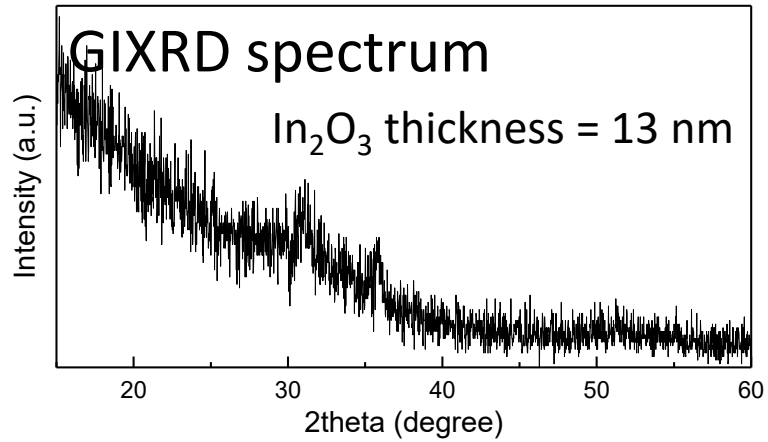
Our approach: plasma-enhanced ALD of In_2O_3



Adapted from Ji, *Appl. Sci. Converg. Technol*. 2019



Stoichiometric ratio:
In : O = 1 : 1.55

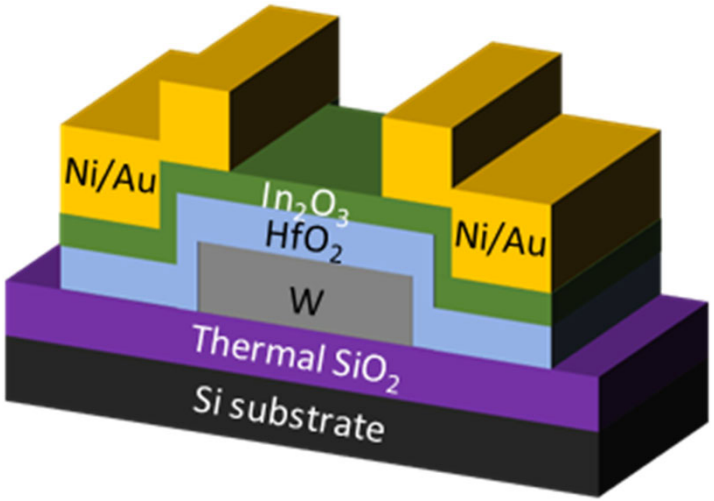


No clear signature of Bragg peaks

XPS and GIXRD carried out by John Huang and Hyungeun Choi at MIT

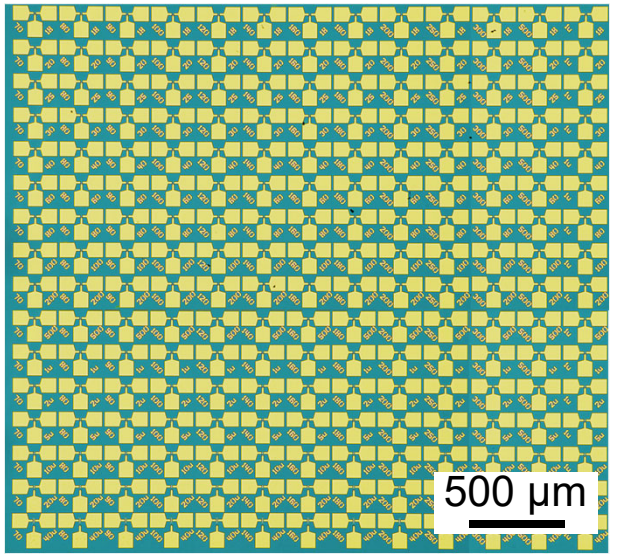
- PEALD uniqueness:
  - Low-*T* growth (150 °C)
  - Low defect density
- Near-ideal stoichiometry
- Amorphous film

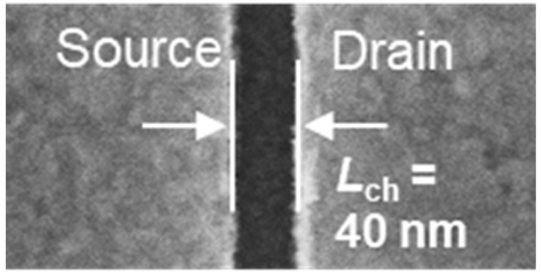
In_2O_3 FETs fabrication



- G sputtering (W)
- HfO_2 by PEALD (250 °C)
- In_2O_3 by PEALD (150 °C)
- S/D Ni/Au contact deposition
- Channel patterning by RIE
- G via opening
- Probe-pad fabrication

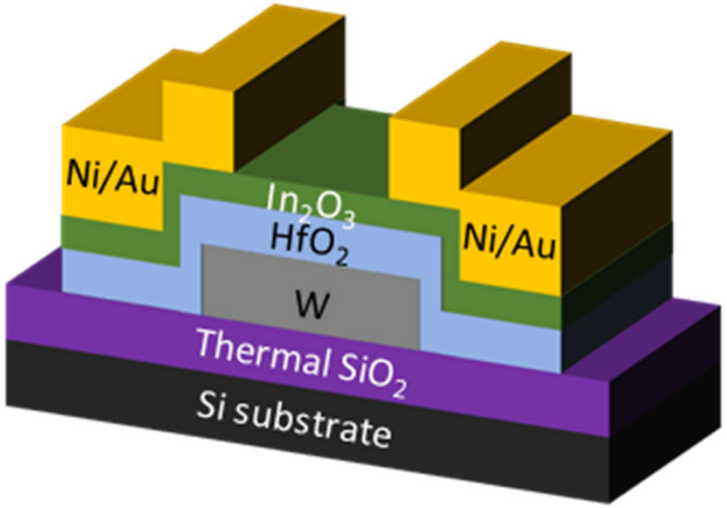
FET array

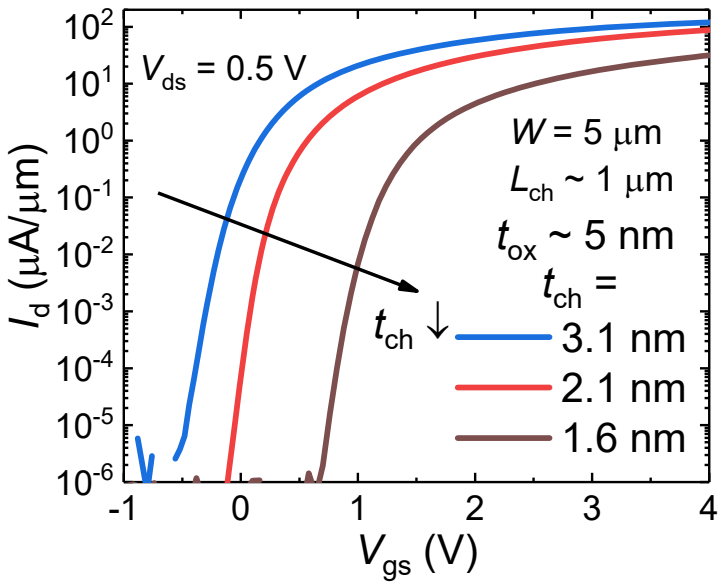


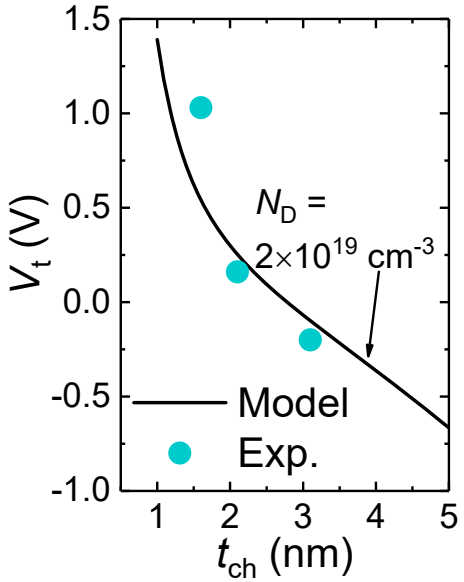


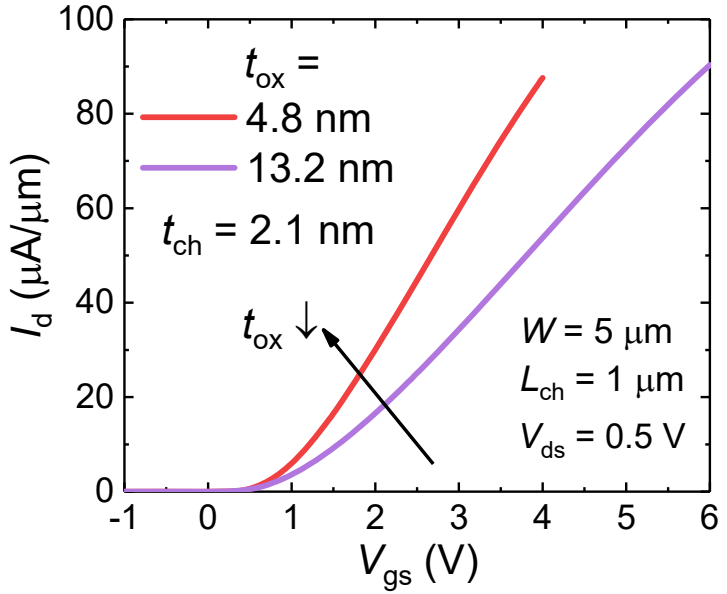
- Process thermal budget = 250 °C
- Critical dimensions: L_{ch} down to 40 nm and W down to 60 nm

V_t control for E-mode FET









Final design:

t_{ch} = 2.1 nm

t_{ox} = 4.8 nm

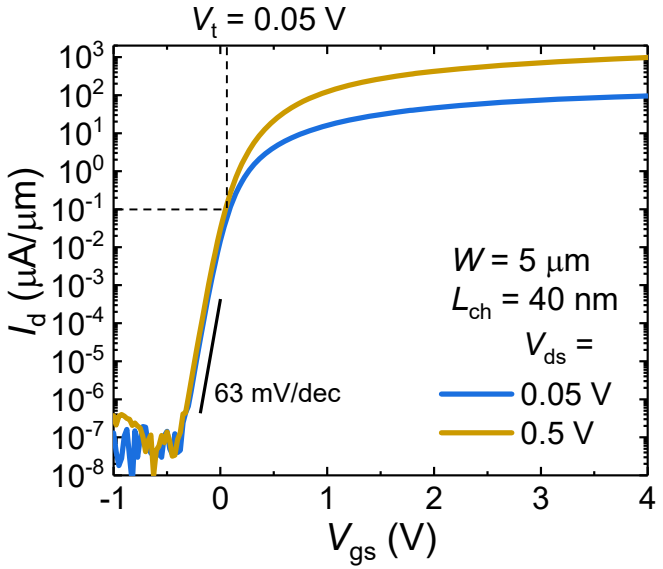
- Balanced V_t and I_{on} at t_{ch} = 2.1 nm
- Scaled gate dielectric thickness for best I_{on}

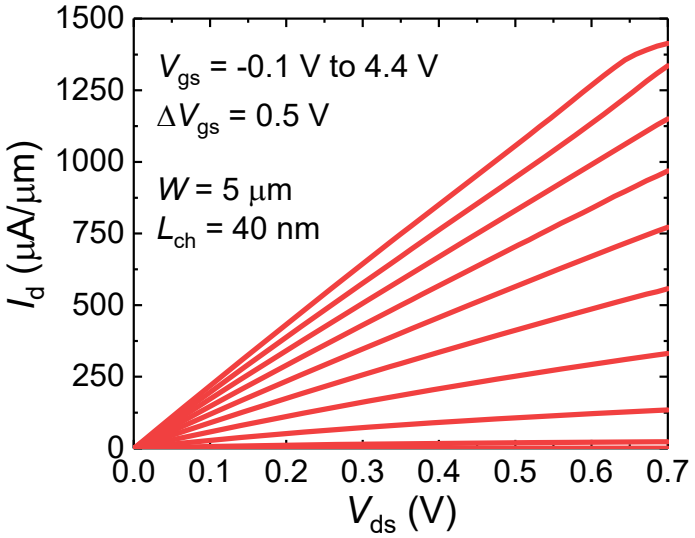
More V_t discussions in:
Liu, *TED* 2024
Jana, *SISPAD* 2024

I-V characteristics of E-mode In_2O_3 FETs

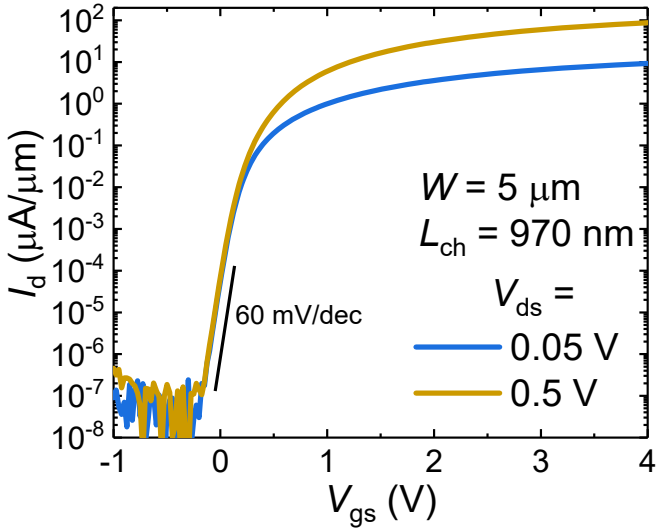
L_{ch} = 40 nm:

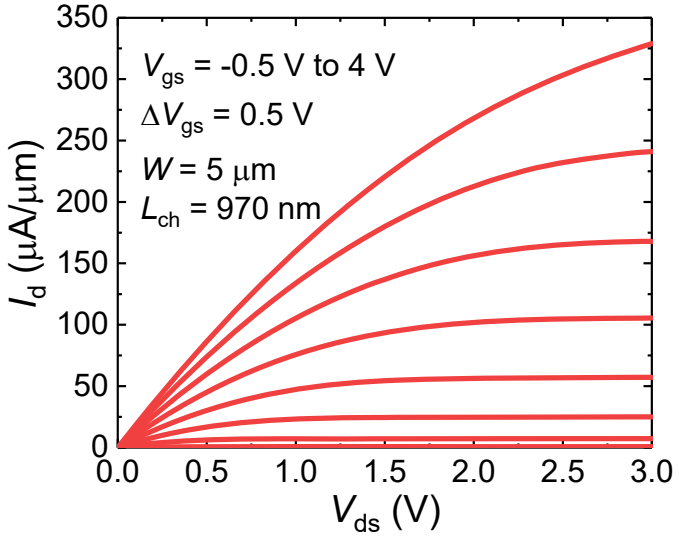
t_{ch} = 2.1 nm
t_{ox} = 4.8 nm





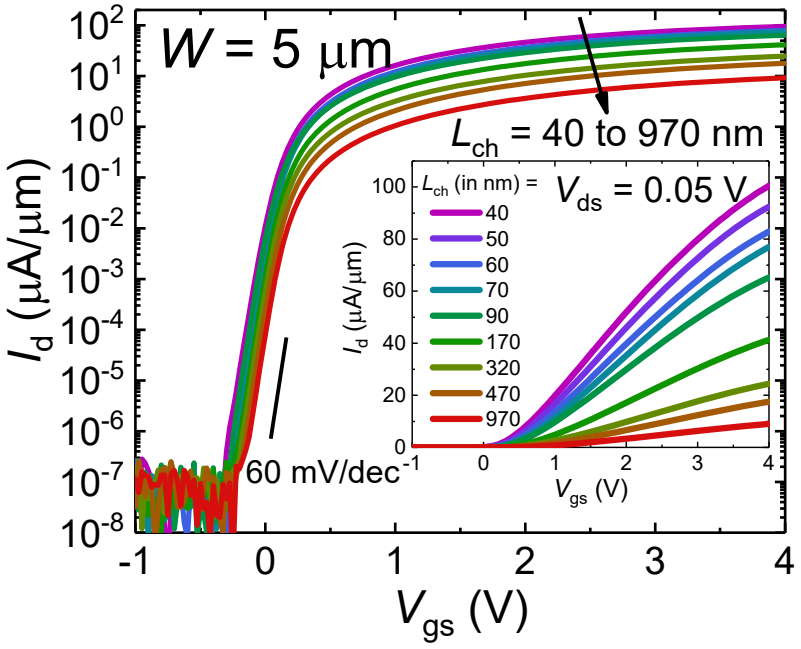
L_{ch} = 970 nm:

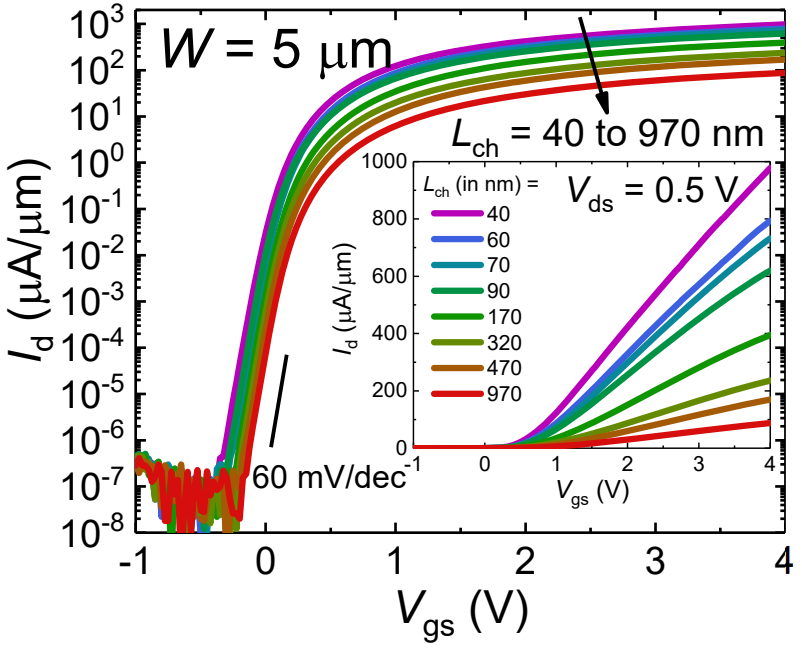


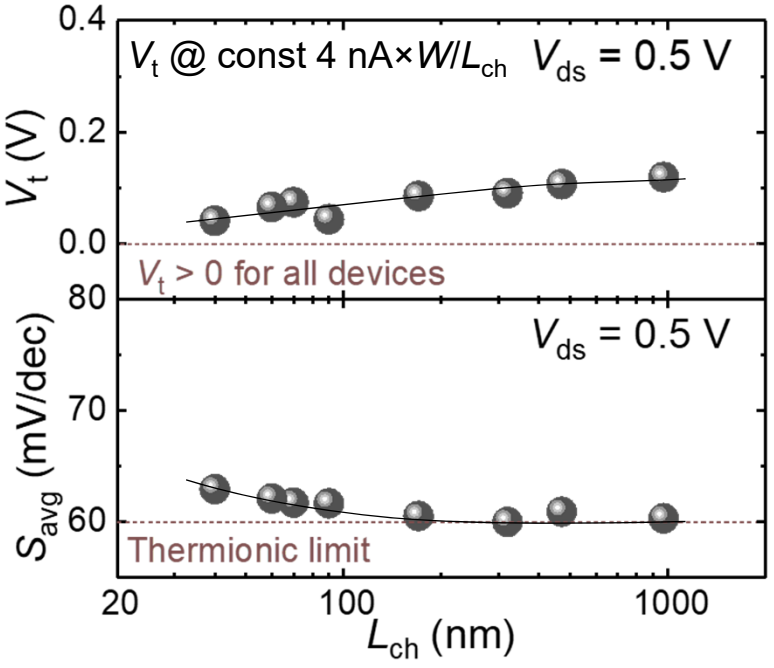


- E-mode in short-channel transistors!
- High I_{on} > 1 mA/μm @ V_{ds} = 0.5 V
- Well-controlled SCEs down to L_{ch} = 40 nm
- Near-ideal *S* down to 60 mV/dec
- Negligible DIBL

Channel length scaling



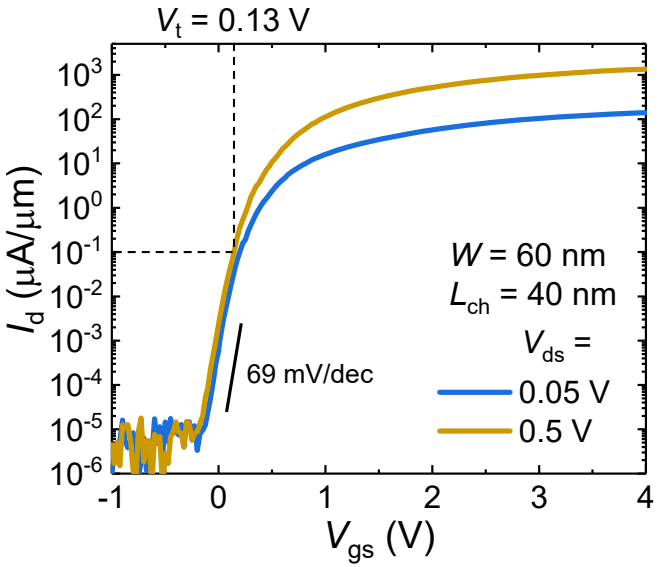


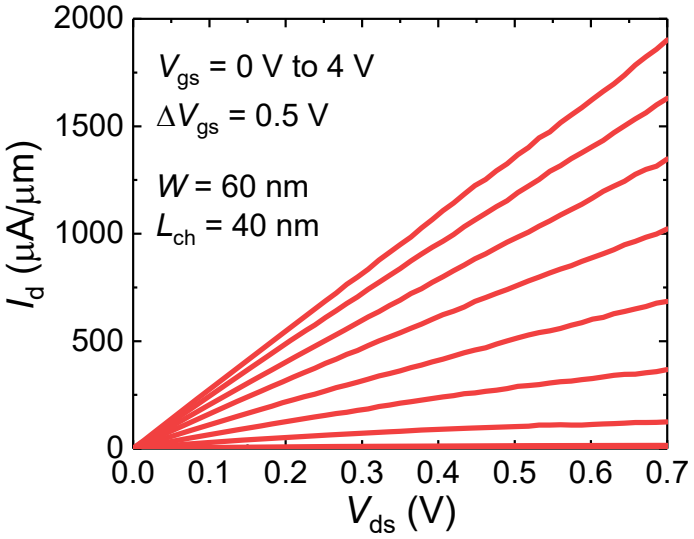


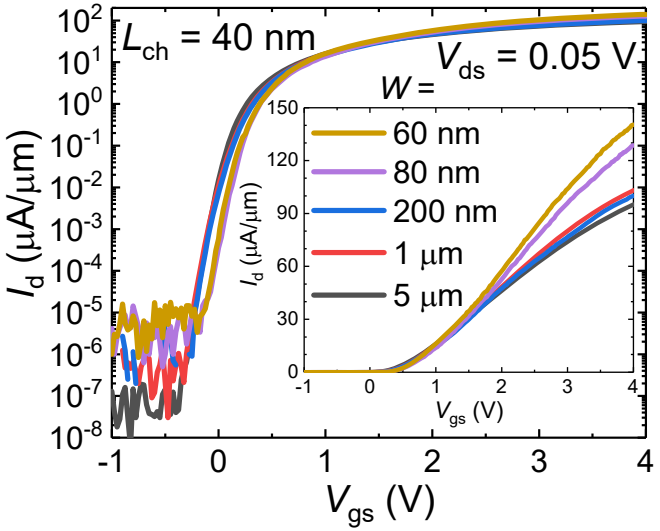
- Negligible V_t roll-off
- Near-ideal S across the full L_{ch} range down to 40 nm

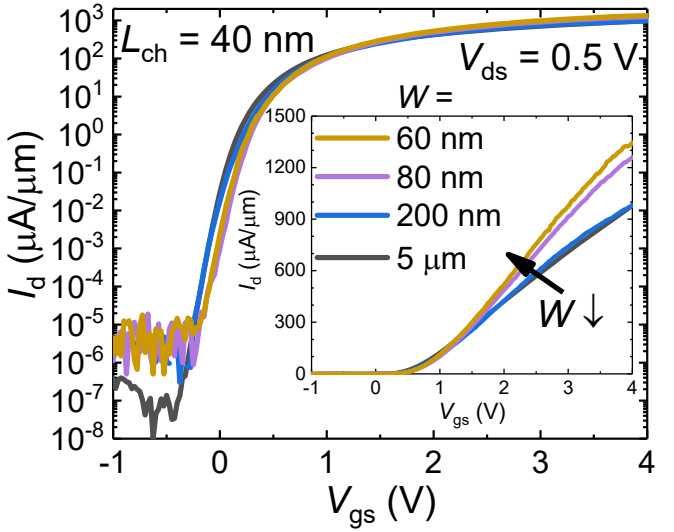
Channel width scaling in short-channel FETs

W/L_{ch} = 60/40 nm:



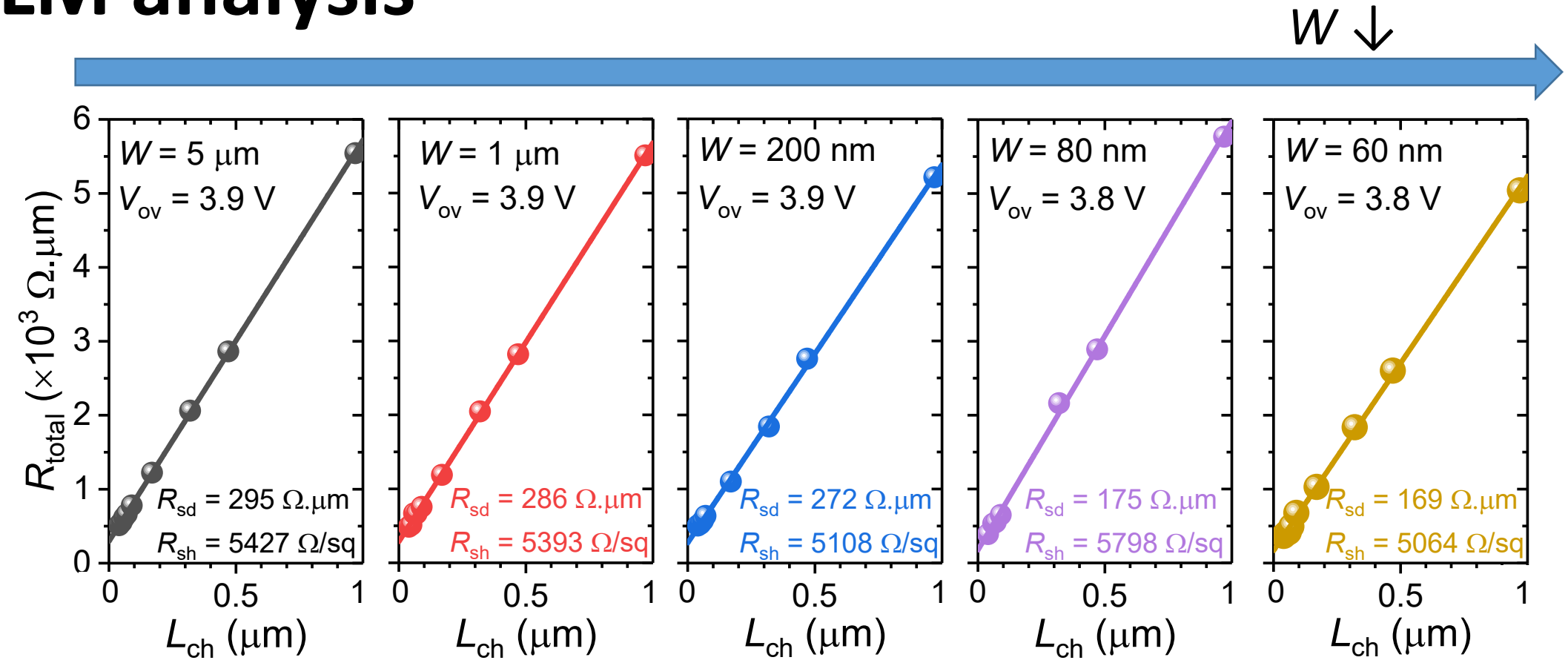






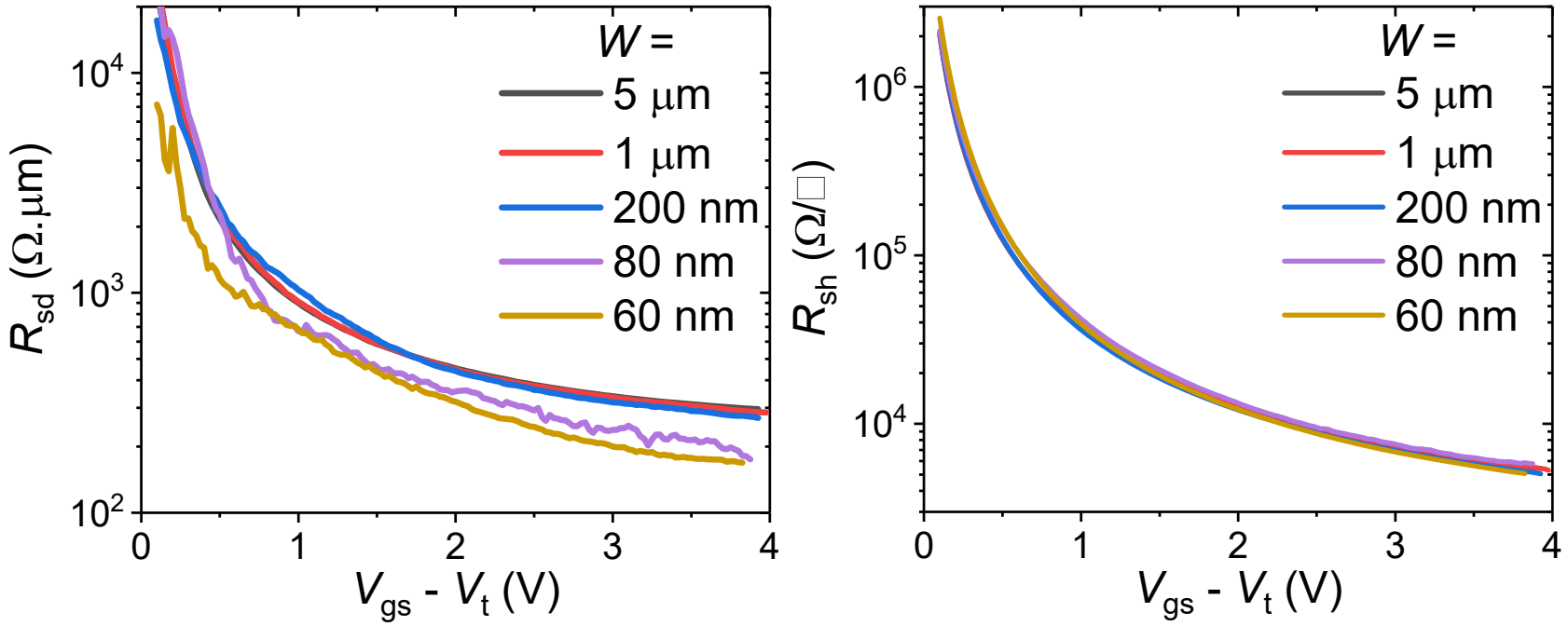
- I_{on} = 1.35 mA/μm @ V_{ds} = 0.5 V
- Negligible SCEs and near-ideal S
- W ↓:
  - $\Delta V_t > 0$
  - I_{on} ↑
  - S nearly unchanged

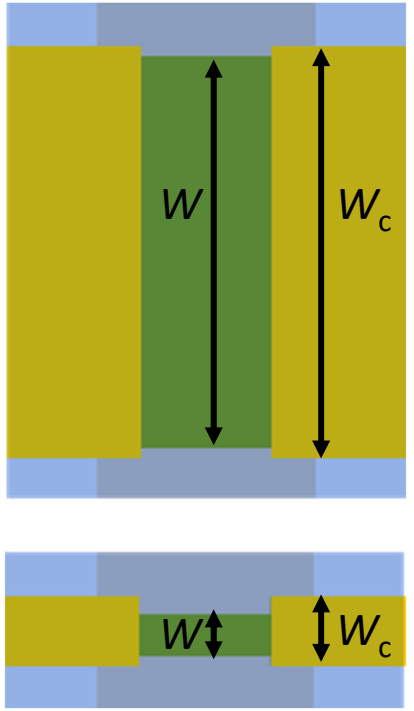
TLM analysis



- Near-ideal linear fittings obtained across all the devices with the full W and L_{ch} range
- Minimum R_{sd} = 169 Ω.μm, record among E-mode AOS-FETs

Contact and sheet resistance

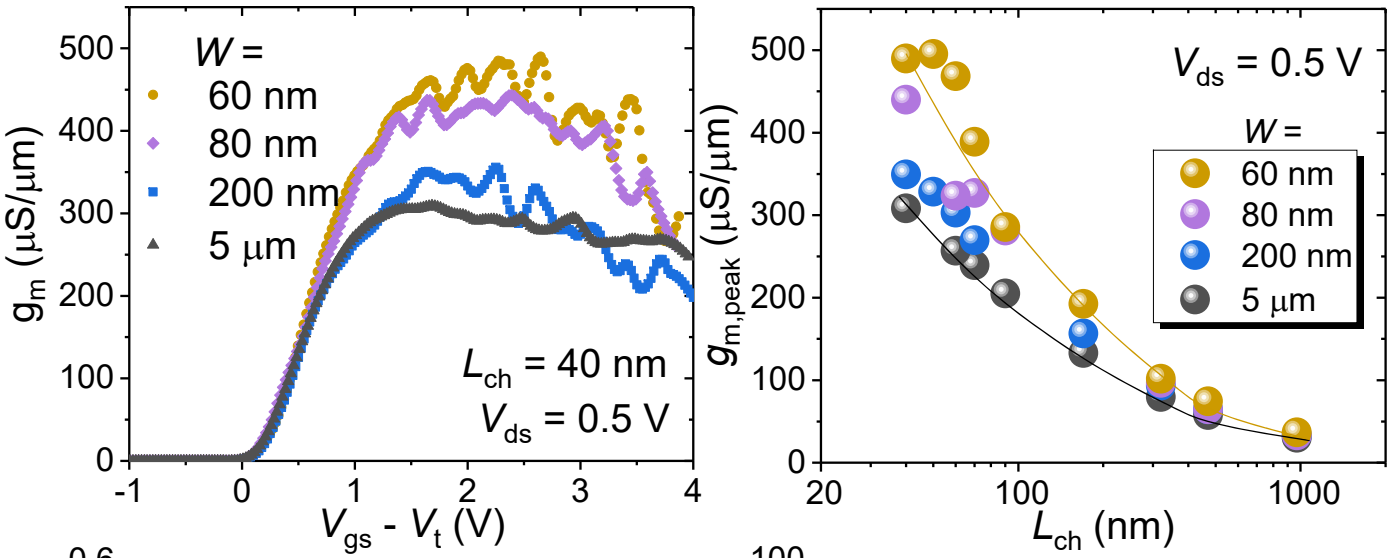


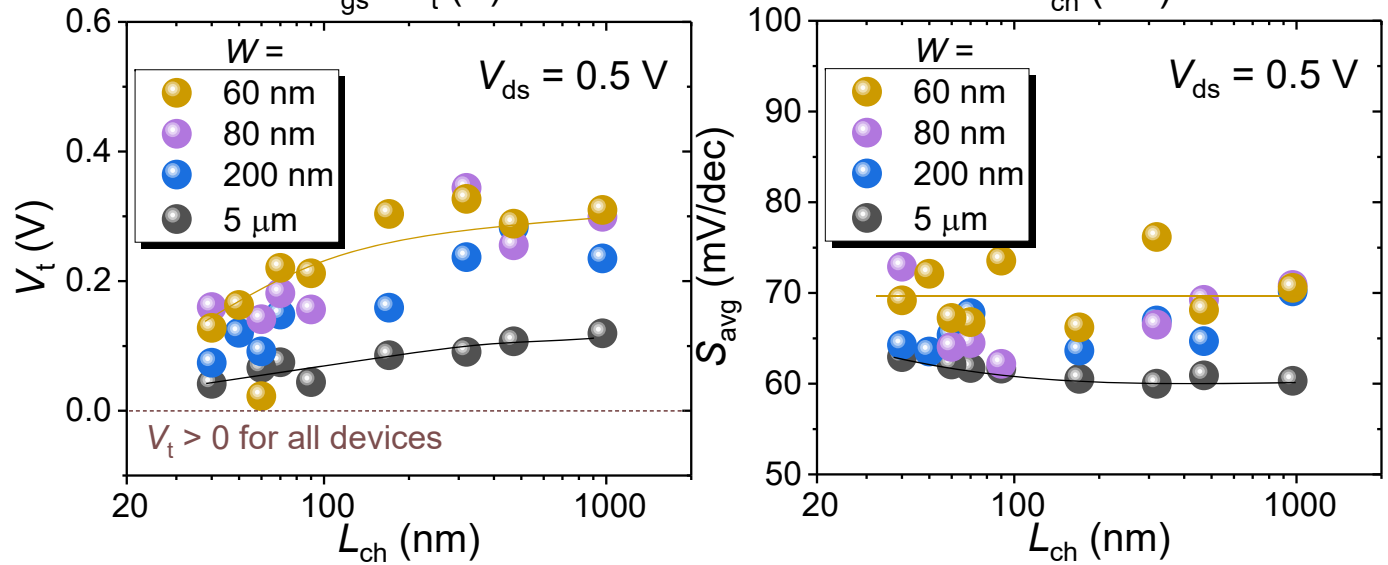


- R_{sd} and R_{sh} heavily depend on V_{gs} (i.e., N_{sheet})
- $W \downarrow$: $R_{sd} \downarrow$, R_{sh} unchanged
- W scaling behavior potentially due to geometry and/or strain effect

Nominal $W_c - W$ = 150 nm for all FETs,
$W_c/W \uparrow$ as $W \downarrow$

Device scaling: key metrics

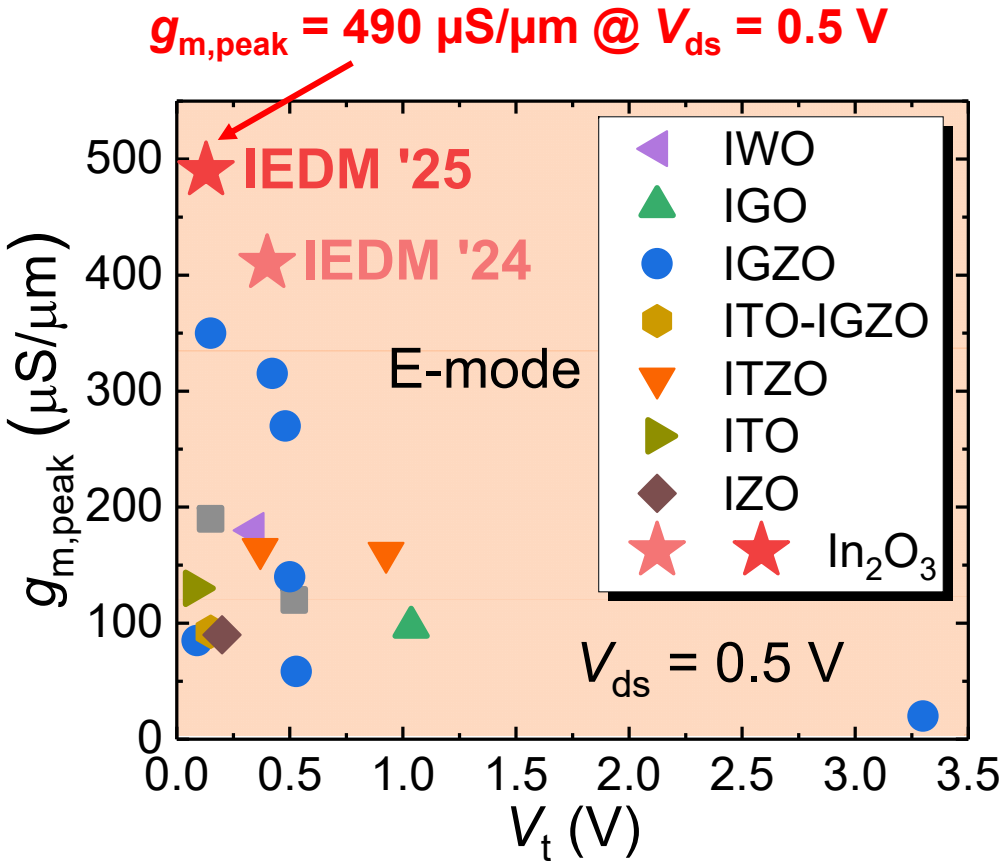


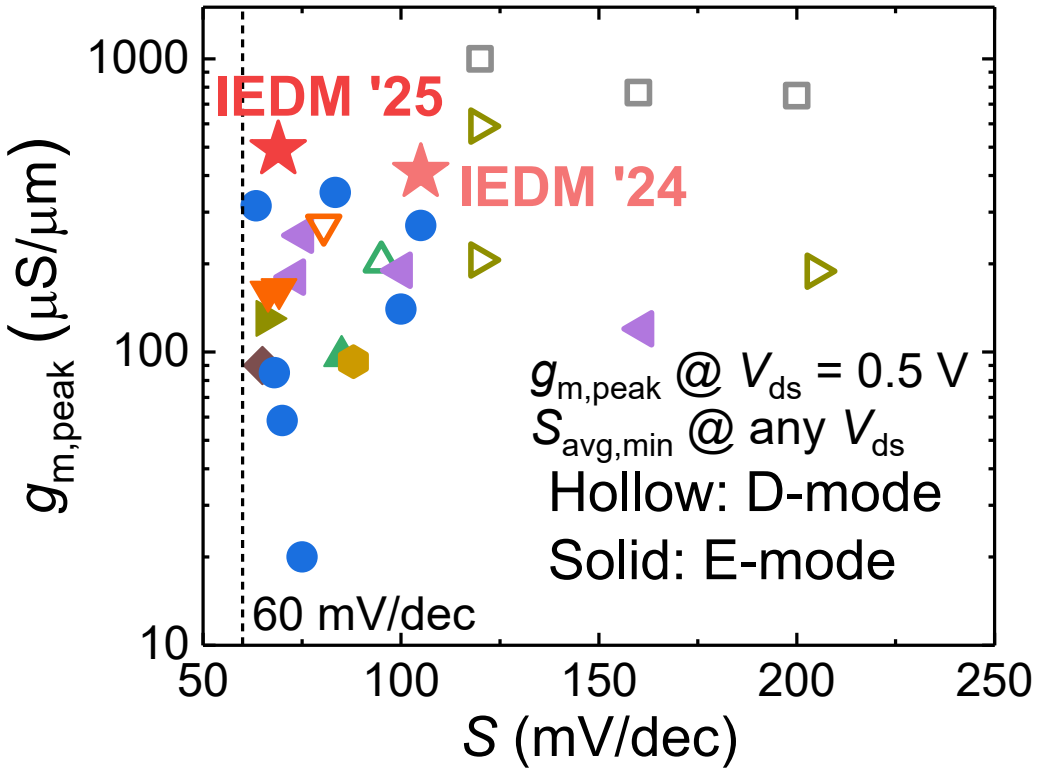


V_t @ const 4 nA×W/L_{ch}

- $W \downarrow$:
  - $g_{m,peak} \uparrow$
  - $\Delta V_t > 0$
  - S nearly unchanged

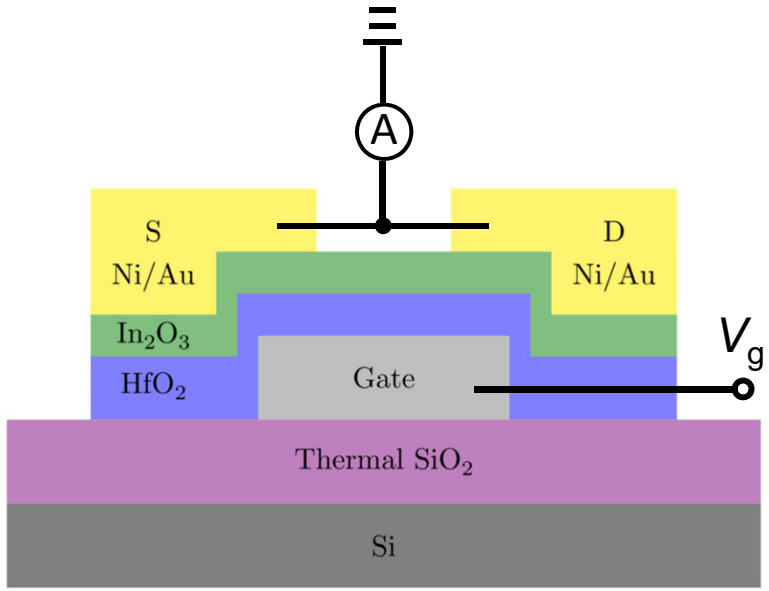
Record logic performance in E-mode oxide FETs

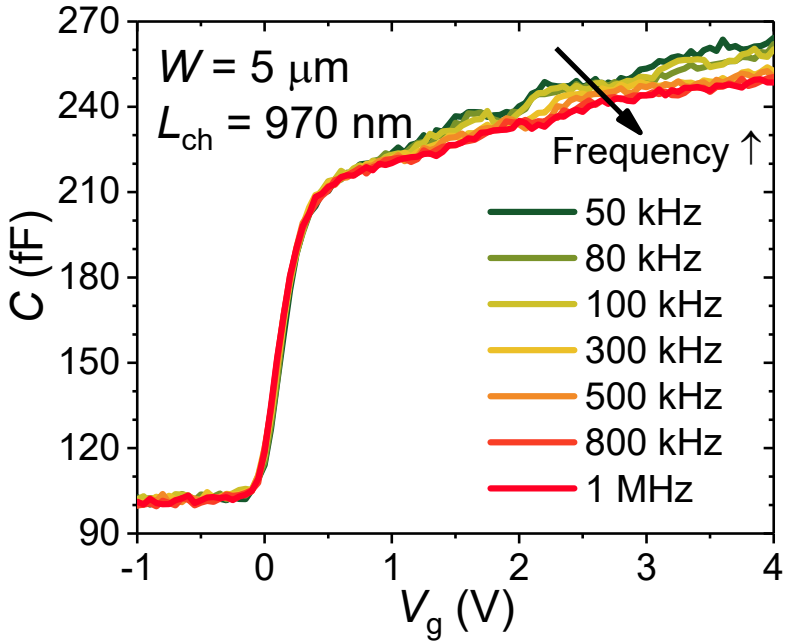


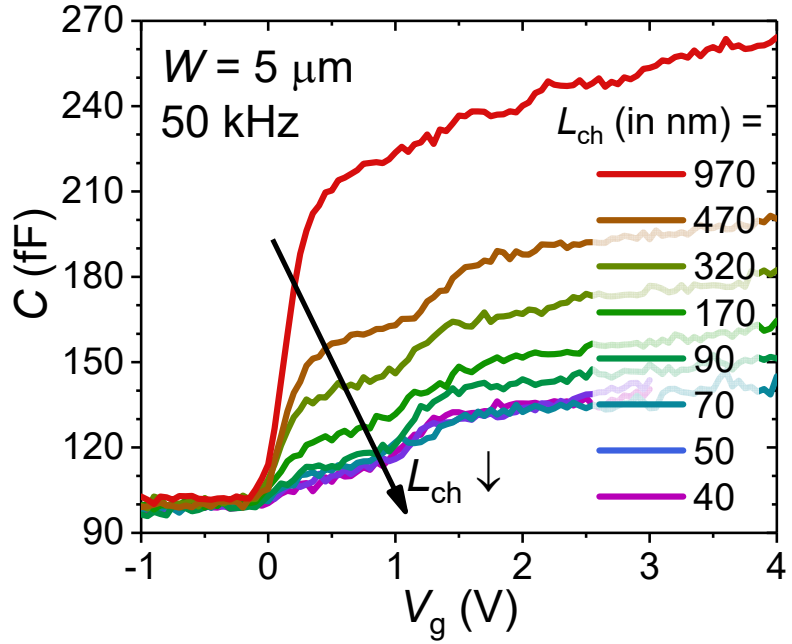


- Record logic performance in E-mode oxide-channel FETs
- Best balanced g_m-S performance in oxide-channel FETs

Capacitance analysis



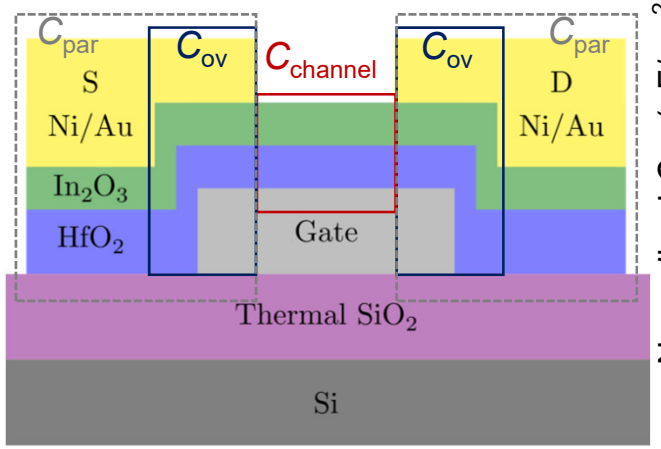




- Nearly no frequency dispersion at low V_g → low trap density in MOS
- L_{ch} ↓:
  - C(V_g < 0) unchanged, mainly due to full depletion under S/D
  - C(V_g > 0) ↓, due to channel and S/D accumulation

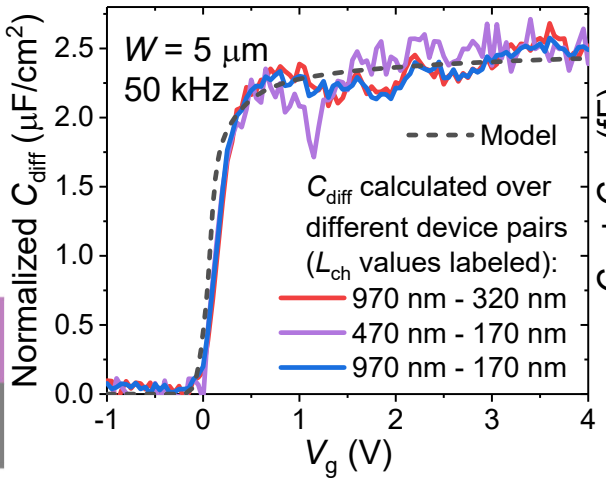
Capacitance components: experiments and modeling

$C_{channel}$ depends on V_g, L_{ch}
C_{ov} depends on V_g
C_{par} constant

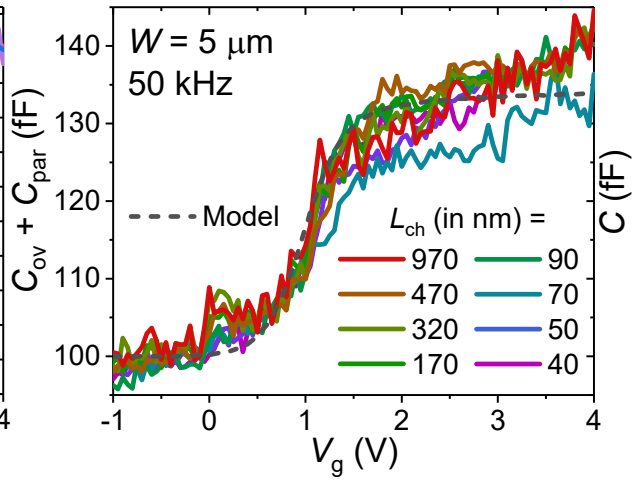


$C_{channel} = WL_{ch}C_{diff}$

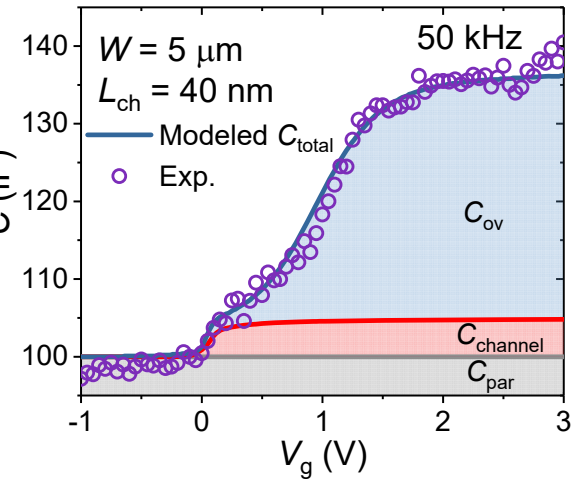
CET = 1.4 nm



C_{ov} + C_{par}

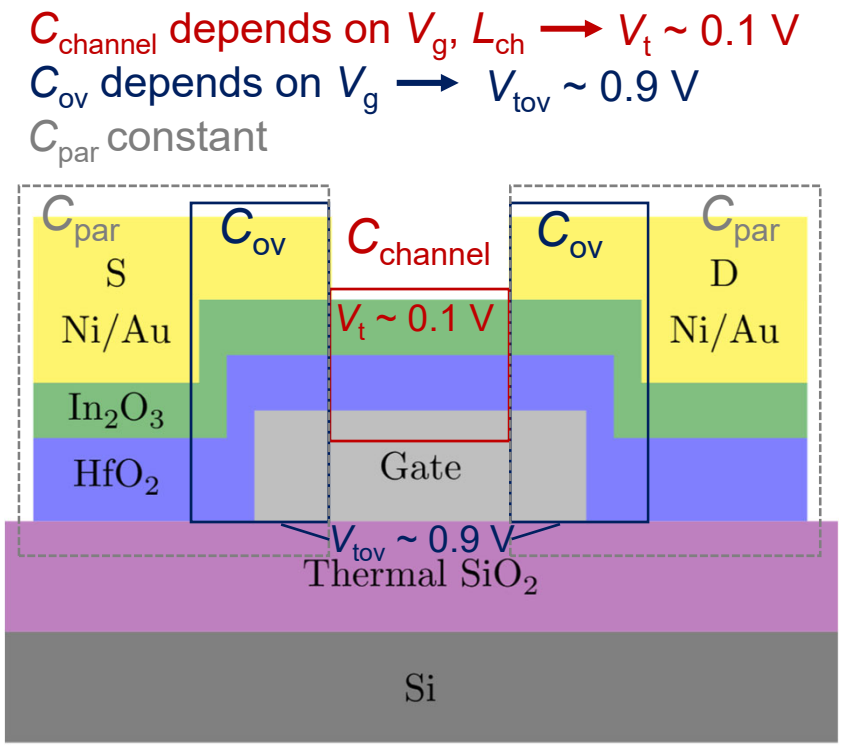


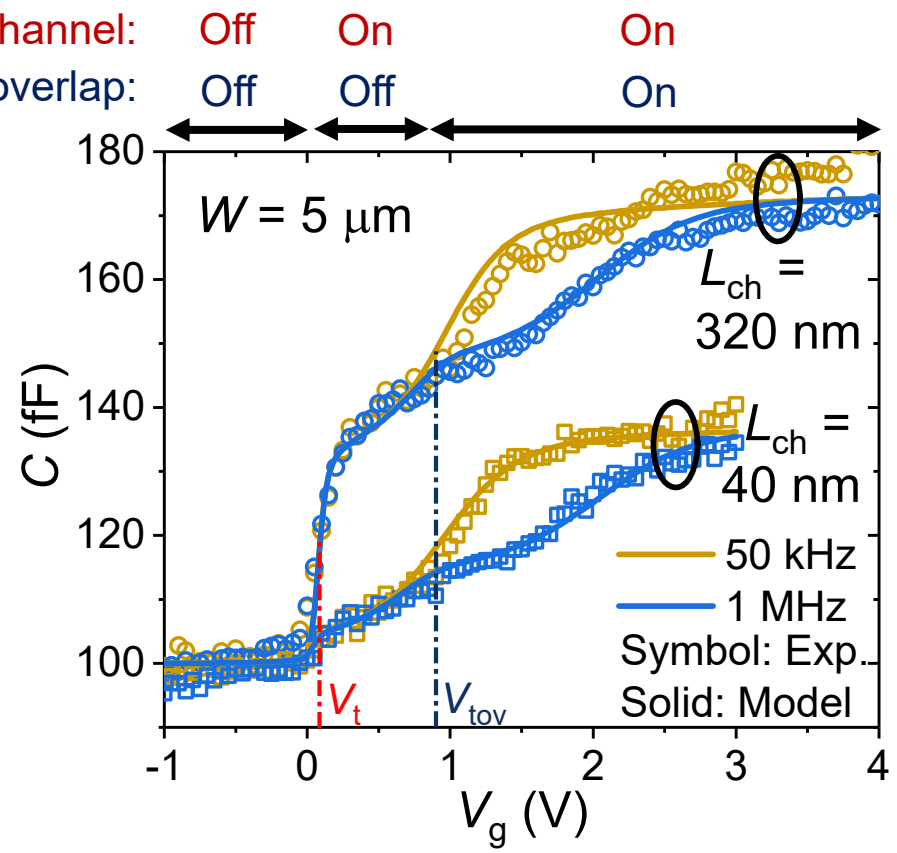
Partitioning of different components



- Accurate extraction of intrinsic channel capacitance
- Separation of L_{ch}-independent components (C_{ov} + C_{par})
- Fitted *C-V* components based on MIT Virtual Source (MVS) model

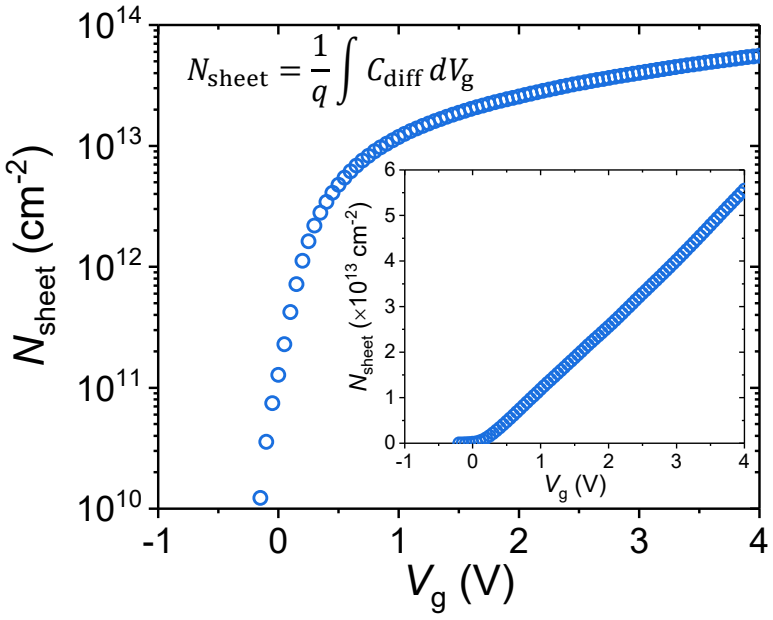
Understanding V_g dependence and f dispersion

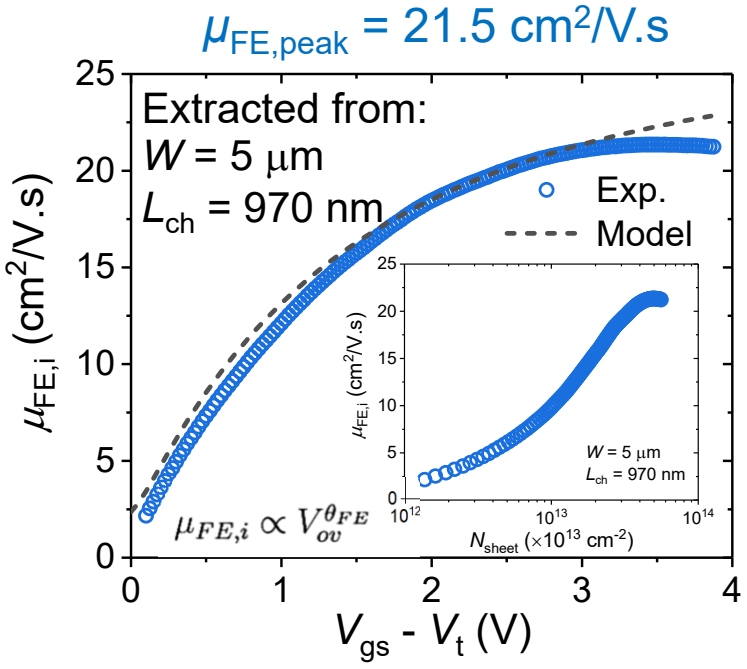




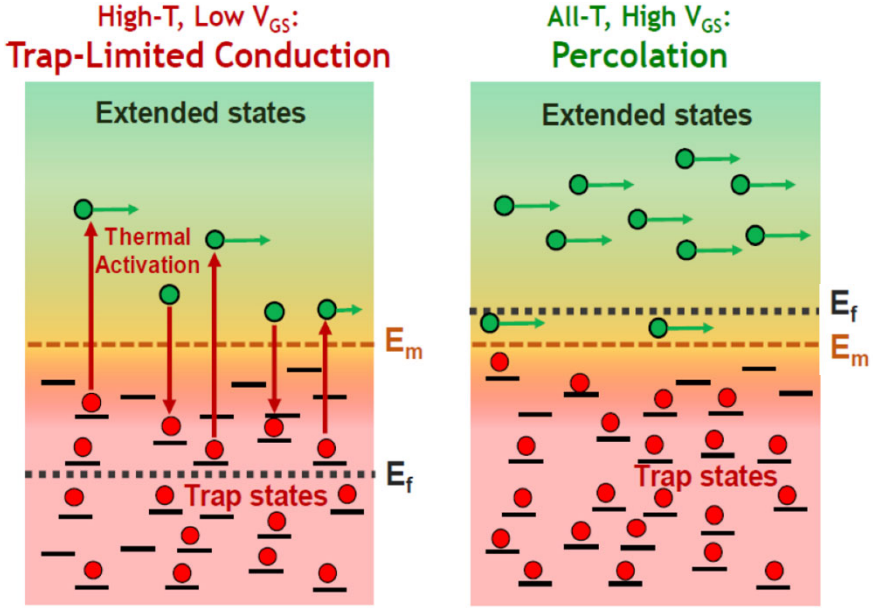
- V_t: intrinsic channel, no frequency dispersion
- V_{tov}: S/D region, frequency dispersion → contact non-idealities

Mobility extraction





- Possible mechanism 1: ionized-dopant screening
- Possible mechanism 2:



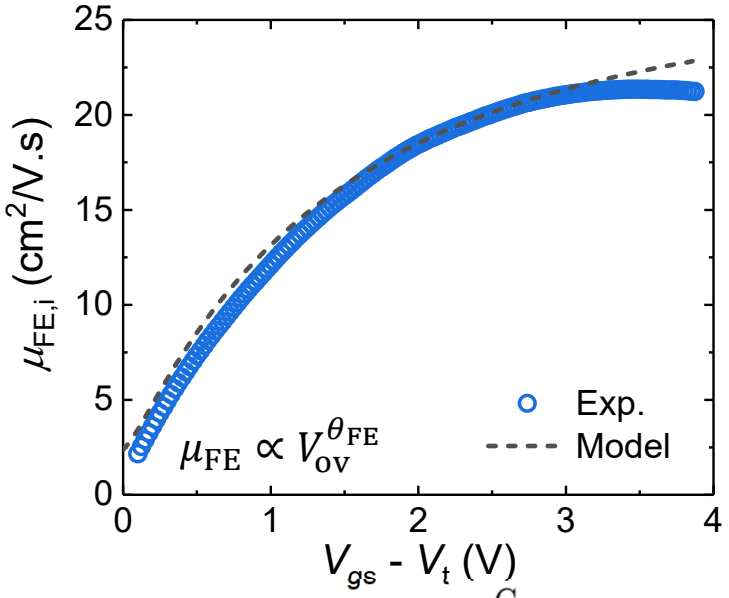
E_m: mobility edge

Chakraborty, *TED* 2020

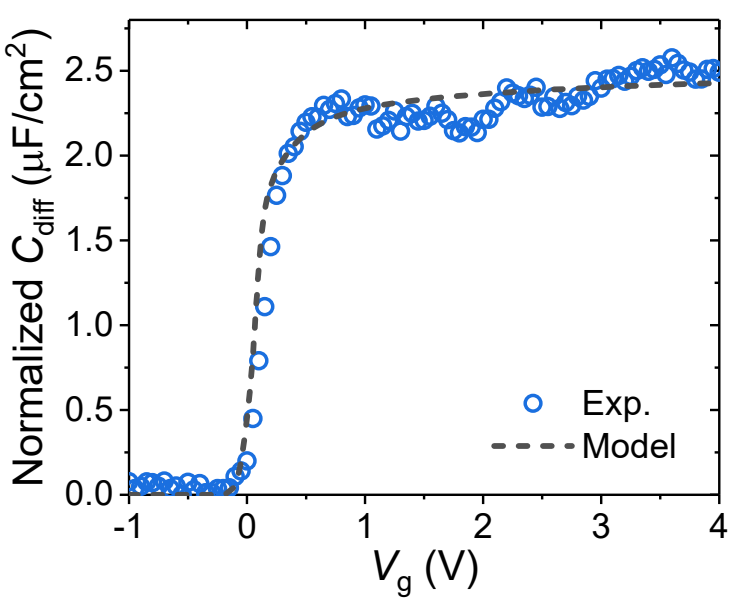
- μ_{FE} strongly depends on N_{sheet}

Key components of compact model MVS-AOS

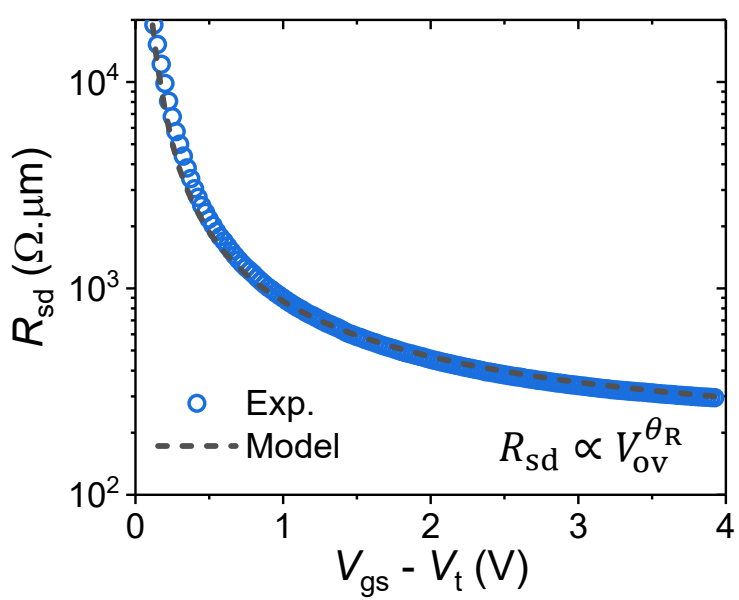
Transport

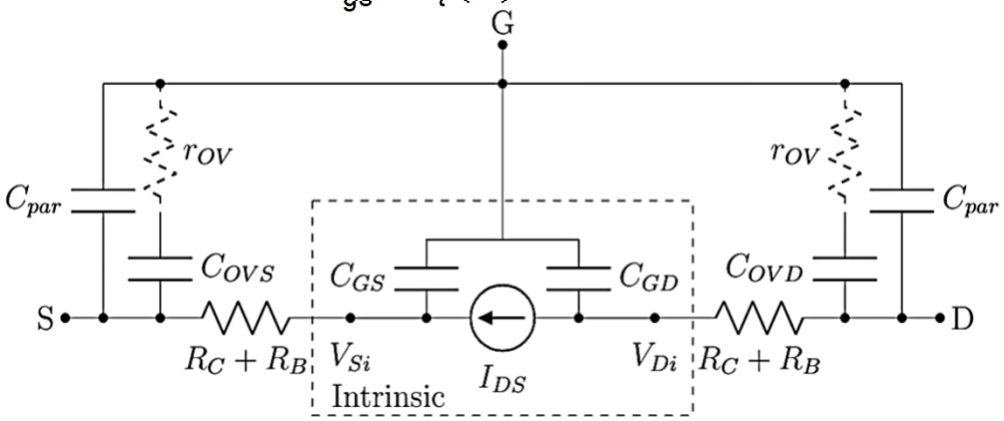


Charge control



Extrinsic resistance



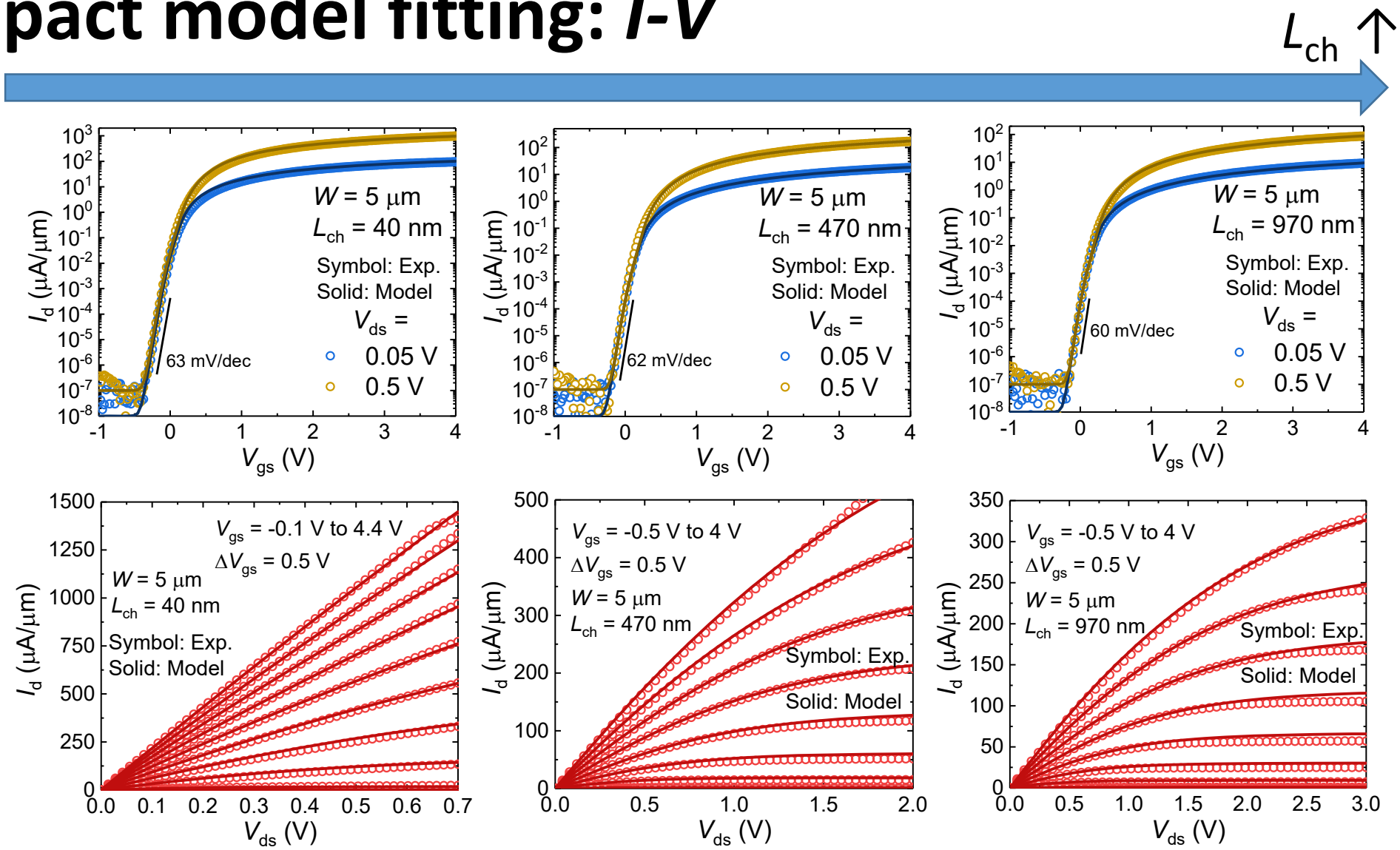


Key elements:
- I_{DS}: intrinsic channel current
- R_B: bias-dep. series R
- R_C: bias-indep. series R
- r_{ov}: small-signal R
- $C_{G(S,D)}$: intrinsic channel C
- $C_{ov(S,D)}$: bias-dep. overlap C
- C_{par}: bias-indep. parasitic C

- Intrinsic channel: drift-diffusion version of MIT Virtual-source Model (MVS) [1,2]
- Extrinsic region

[1] Radhakrishna, *TED* 2019; [2] Wei, *BCICTS* 2024

Compact model fitting: *I-V*

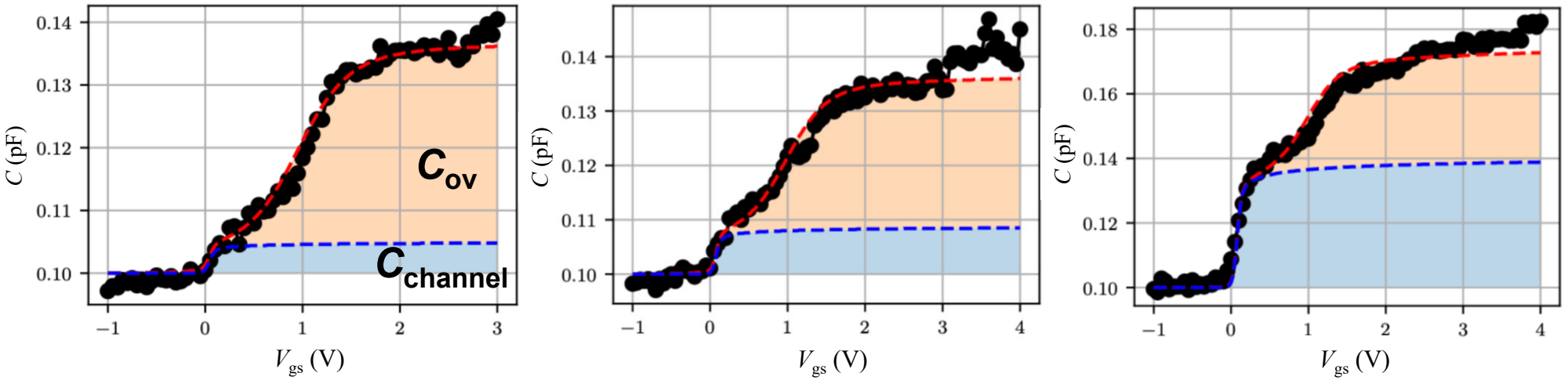


- Reproducible fitting across the full L_{ch} range with identical parameters!

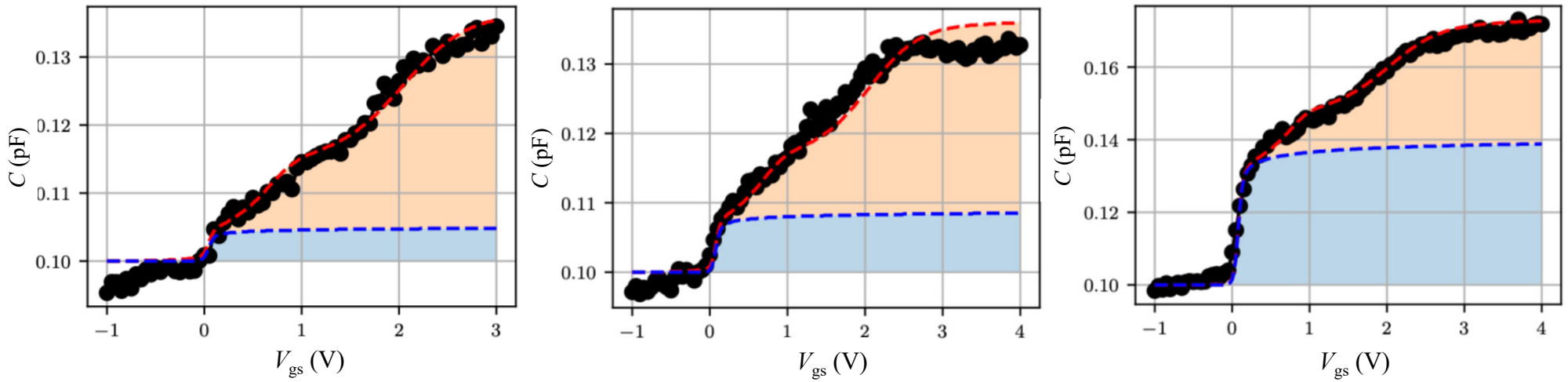
Compact model fitting: *C-V*

L_{ch} ↑

50 kHz:



1 MHz:



- Reproducible fitting across the full L_{ch} range with identical parameters!

Conclusions

- E-mode BEOL AOS-FETs with record logic performance
- Near-ideal scaling realized in BEOL In_2O_3 FETs
- Detailed study of capacitance reveals unique physics
- Development of the MVS-AOS compact model

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